IN THE DRAWINGS

Please amend Figs. 1 and 2 by adding reference numerals, changing certain dashed lines to solid lines, and adding to Fig. 1 certain elements shown in Fig. 2 (and *vice versa*), as indicated in the attached REPLACEMENT SHEETS and described in detail in the REMARKS section of this response.

REMARKS

Reconsideration of the application is respectfully requested for the following reasons:

1. Amendments to Drawings

Portions of Figures 1 and 2 have been amended to include conventional notations for word lines and bit lines, in order to facilitate understanding of the invention. In addition, the drawings have been amended to overcome the objections set forth on pages 2 and 3 of the Official Action, as described in more detail below.

The amendments to Fig. 1 are based on the description on page 2, lines 14-23 of the original specification, and use notations similar to those used in U.S. Patent No. 6528837. The amendments to Fig. 2 correspond to those made to Fig. 1, and to the description on page 2, lines 24-25 of the original specification. Consequently, it is believed that the amendments do not introduce "new matter."

In amended Fig. 1, two bit lines 11 are amended to bit lines 11a and 11b for accurately illustrating the present invention, and are shown with dashed lines because bit lines 11a and 11b are not yet formed until at least the electrical test is accomplished. Since a bit line contact window is conventionally placed in the active area to make contact with a bit line, the bit line contact windows 16, 16', and 16" are added in the active areas 13, 13', and 13", respectively, to make contact with bit line 11a or 11b.

In addition, in Fig. 1, the gate G, source S, and drain D are labeled, and the oval elements overlapped with deep trenches 15 have been removed since the overlapping oval elements are unnecessary structure for the present invention.

Finally, reference number 12 has been amended to represent the word lines to more accurately show the structure of the present invention, and the frames of deep trenches 15 are

amended from solid lines to dashed lines to specifically show that the deep trenches 15 are not connected with the gates G. Also, the cross-section line A-A has been adjusted to intersect the deep trenches 15 for matching the section shown in Fig. 2.

Amended Fig. 2 is the longitudinal sectional diagram taken from the cross-section line A-A in the amended Figure 1. In amended Fig. 2, dashed lines have been added to represent the vertical cross-section line A-A shown in Fig. 1; the dotted regions S below and between each G have been added to indicate the sources, and regions D to indicate the drains; the horizontal shaded bars 19 directly underlying Gs of area 13' have been added to indicate the top trench oxide and the vertical shaded bars 20 to indicate the collar oxide; long horizontal bars 21 have been added to indicate the buried plate; and WL has been amended to gate G for matching the structure shown in amended Fig. 1.

Furthermore, structures 13, 13', and 13" in amended Fig. 2 are amended into two parts: the upper part containing regions 11a, 11b, 12, and 18c, and the lower part containing regions 16, 16', 16", 18a, and 18c to illustrate the longitudinal sectional structure taken from the cross-section line A-A in the amended Fig. 1. Upper part contains 11a and 11b to indicate the bit lines, 12 indicates the word lines, and 18c indicates the insulators; lower part contains 16, 16', and 16" indicates the bit line contact windows and structures 18a and 18b indicate the insulators. The frames of bit lines 11a and 11b are shown with dashed lines to match that shown in Fig. 1 because the bit lines are not yet formed until the electrical test to the device is accomplished. In addition, the shape of gates G right below 18b have been trimmed for matching the cross-sectional view along the cross-section line A-A in Fig. 1.

It is respectfully noted that the amendments made in Figs. 1 and 2 have been made for the purpose of improving the clarity of the description and do not touch upon the features of the present invention.

The specific objections to the drawings set forth on pages 2-3 have therefore been overcome, as follows:

- The ovals overlapping elements 15 in Fig. 1 have been removed from the drawing since the overlapping oval elements are unnecessary structure for the present invention and obscure the patentable features.
- Labels have been added to Fig. 2 to show that:
  - the dotted regions just below and between each "WL" (now amended to "G") are sources S (below 16 and 16") and drains D (below 16' and next to 15) ;
  - horizontal shaded bars directly underlying "WL"s of area 13' are top trench oxide 19;
  - vertical shaded bars on either side in the upper portion of trenches 15 are collar oxide 20; and
  - long horizontal bars under said vertical shaded bars and outside trenches 15 are buried plate 21.
- The reference character "12" has been amended from gate to word line and "WL" has been amended to "G" as gate, to more accurately define the structure of the present invention in accordance with convention.
- The active areas 13, 13', and 13" in Fig. 2 have been amended and specifically distinguished into two parts: the upper part containing bit lines (11a and 11b), word lines (12), and insulators (18c), and the lower part containing bit line contact windows (16, 16', and 16") and insulators (18a and 18b) for matching the structure shown in Fig. 1, according to the conventional art that the bit lines are generally formed above the gates, drains, and sources, and make contact with them via bit line contact windows.

Since the elements in Fig. 1 are further labeled and defined, and Fig. 2 has been amended in accordance with convention for matching with Fig. 1, both drawings are now consistent, thereby overcoming the objection set forth on page 2 of the Official Action.

1. Amendments to Specification

The specification has been amended to be consistent with amended Figs. 1 and 2 and the amended claims, to more clearly describe the features of the present invention, and to overcome specific objections made on page 4 of the Official Action, as follows:

Page 1, lines 30-32 and page 2, lines 1-6 have been amended to refer to adjacent bit lines and first and second active areas, as shown in the original drawings and now recited in the claims.

Page 2, lines 25-26, have been amended to more clearly describe the relationship between the bit lines 11a and 11b, in accordance with Fig. 1 of the present invention. Conventionally, a cell has a source, a gate, and a drain, and therefore page 2, lines 30-31, now describes "A source S ...a cell in the present invention." In addition, page 2, lines 31-32, have been amended to include a detailed description regarding to the relationship between the active areas, the cells, and the word lines, in order to more fully describe the structure of memory device shown in Fig. 1 of the present application.

In amended specification page 2, line 32 and page 3, lines 1-2, conventionally a bit line contact window is placed in the active area to make contact with a bit line. As a result, the description "Generally, ... later developed bit lines 11a and 11b" has been provided. Similarly, in amended specification page 3, lines 8-12, the function of the present invention "word line 12... deep trench 15 to the word lines 12..." is further provided to more specifically describe how the GIDL current and junction leakage current are measured, according to the original content of the specification page 1, lines 14-16 and page 2, lines 22-23. In amended specification page 3, lines 14-15, "... wherein two dashed lines ... shown in Fig. 1;" is added to provide detailed descriptions for the structure shown in Fig. 2, and in amended specification page 3, lines 15-21, the description "...G indicates a gate... 21 are buried plate." is provided to fully describe each element of the device structure shown in Fig. 2 of the present invention.

In amended specification page 2, line 24, reference number 11 is amended to 11a and 11b, and gate 12 is amended to word line 12. On page 2, lines 27-28, the relationship between the active areas 13, 13', and 13" and the bit lines 11a and 11b are more specifically described according to Fig. 1 of the present invention.

Finally, in amended specification page 3, lines 4-7, the relationship between the deep trenches 15, the cells, and the active areas 13, 13', and 13" is more specifically described based on Fig. 1 of the present invention. On page 3, line 15, WL is replaced by gate G in order to be more consistently with terminology used by those skilled in the art.

The specific objections to the specification in the official action page 4 have been addressed as follows:

- The identified elements of Fig. 2 for which labels have been omitted are provided in the amended specification page 3, lines 15-21 "... G indicates a gate... are buried plate";
- The gates "12" on page 2, line 24 and in Fig. 1 have been amended to word line "12"; word lines "WL" on page 3, line 15 and in Fig. 2 have been amended to gates "G" for matching Figs. 1 and 2, according to convention;
- Further descriptions of active areas 13, 13', and 13" are provided on page 2, line 32 and on page 3, lines 1-2 "Generally... later developed bit lines 11a and 11b.", also the amendment of structures 13, 13', and 13" in Fig. 2 have been made and the labels of the amended structures have been provided (see corresponding amendment to drawing above).

According to the descriptions above, the specification has been amended to meet the requirements for the specification as set forth on page of the official action. Thus, withdrawal of the objection to the specification is respectfully requested.

3. Objections to Claims

This objection has been rendered moot by the cancellation of claims 1 and 2.

In addition, it is respectfully noted that, in claim 4, "a plurality of gates...;" has been changed to "a plurality of word lines...;" to more accurately define the structure of the present invention.

4. Claim Rejections – 35 USC § 102

Claim 4 of the present invention have been amended as shown above to more specifically define the structure of the present invention according to Figs. 1 and 2, since generally a cell has a gate, a source, and a drain. Based on original Figs. 1 and 2, it can be seen that each of the active areas 13, 13', and 13" contains two cells, which share a bit line 11a, so that each active area is connected to one bit line 11a or 11b, as is now recited in claim 4. Deep trench 15 is connected to two cells of two different active areas 13 and 13', which means deep trench 15 is connected to two word lines 12 since each cell communicates to a word line 12, as also recited in claim 4. These features are not anticipate by U.S. Patent No. 6,198,151 (Wada).

In accordance with Fig. 3 of the Wada patent, which is an equivalent circuit diagram of the memory cell array of the DRAM shown in Fig. 1 of Wada, a cell is defined to contain a deep trench C1 and two different active areas Tr11 and Tr12, which are respectively connected to bit lines BL1 and BL1', and a cell is connected to one word line WL1. According to Fig. 3 of Wada, therefore, the corresponding cell shown in Fig. 2 of Wada contains deep trench 202 and two active areas 111 and 112. One cell is connected to one word line WL1, which means deep trench 202 communicates exclusively with **one** word line WL1. In one cell there are two active areas 111 and 112, each of which is respectively connected to the bit lines BL1 and BL1'.

According to the description above, the memory cell of Wada contains a deep trench 202 and two active areas 111 and 112, while the memory cell in the present invention contains a gate, a source, and a drain. The active areas 111 and 112 of Wada are located in one cell and each

active area is connected to one bit line BL1 or BL1', which makes one cell connect to two bit lines BL1 and BL1', while each of the active areas 13, 13', and 13" of the present invention contains two cells and these two cells share a bit line 11a or 11b. The deep trench 202 of Wada is located in one cell and connects to one word line WL1, while the deep trench 15 of the present invention is connected to two different cells that are respectively located at two different active areas 13 and 13', or 13' and 13", and each cell is connected to one word line 12, which makes each of the deep trenches 15 connect to two word lines 12.

Therefore, the semiconductor memory device structures of the present invention and Wada are clearly distinguishable, and neither claim 4 nor dependent claim 5 can be said to be anticipated by the Wada patent. Accordingly, withdrawal of the rejection of claims 4 and 5 in view of the Wada patent is respectfully requested.

Having thus overcome each of the rejections made in the Official Action, expedited passage of the application to issue is requested.

Respectfully submitted,

BACON & THOMAS, PLLC

Date: February 2, 2007

By: BENJAMIN E. URCIA
Registration No. 33,805

BACON & THOMAS, PLLC
625 Slaters Lane, 4th Floor
Alexandria, Virginia 22314

Telephone: (703) 683-0500

NWB:S:\Producer\bert\Pending A...H\CCHANG 718666\a05.wpd